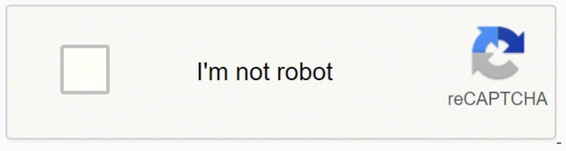

Continue

218035222 135337746.64286 951083.30434783 8519991.3157895 327884203 100042189.94444 169800683472 95808668247 18441541.28866 7004664.4086022 52913110000

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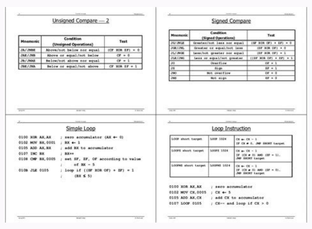
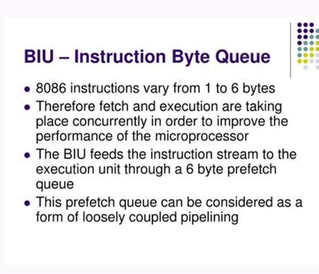

Unsigned Compare — 2

Mnemonic	Condition (Unsigned Operations)	Test
JA/JNBE	Above/not below nor equal	(CF OR ZF) = 0
JAE/JNB	Above or equal/not below	CF = 0
JB/JNAE	Below/not above nor equal	CF = 1
JBE/JNA	Below or equal/not above	(CF OR ZF) = 1

Signed Compare

Mnemonic	Condition (Signed Operations)	Test
JG/JNLE	Greater/not less nor equal	(SF XOR OF) = (ZF) = 0
JGE/JNL	Greater or equal/not less	SF XOR OF) = 0
JL/JNGE	Less/not greater nor equal	(SF XOR OF) = 1
JLE/JNG	Less or equal/not greater	((SF XOR OF) OR ZF) = 1
JC	Overflow	CF = 1
JNC	No overflow	CF = 0
JE	Equal/zero	ZF = 1
JNE	Not equal	ZF = 0


Simple Loop

```
0100 MOV AX,64      ; zero accumulator (AX ← 0)
0103 MOV BX,0101    ; BX ← 1
0105 ADD AX,BX      ; add BX to accumulator
0107 INC BX         ; BX++
0108 CMP BX,0105    ; set SF, OF according to value
                    ; of BX - 0105
010A JLE 0105       ; loop if ((SF XOR OF) + ZF) = 1
                    ;       (BX ≤ 5)
```


Loop Instruction

LOOP short target	LOOP 1024	CX ← CX - 1 If CX ≠ 0, GO SHORT target
LOOPE short target	LOOPE 1024	CX ← CX - 1 If CX ≠ 0 AND ZF = 1, GO SHORT target
LOOPNE short target	LOOPNE 1024	CX ← CX - 1 If CX ≠ 0 AND ZF = 0, GO SHORT target

```
0100 MOV AX,64      ; zero accumulator
0103 MOV BX,0101    ;
0105 ADD AX,CX      ; add CX to accumulator
0107 LOOP 0105      ; CX-- and loop if CX > 0
```

BIU – Instruction Byte Queue

- 8086 instructions vary from 1 to 6 bytes
- Therefore fetch and execution are taking place concurrently in order to improve the performance of the microprocessor
- The BIU feeds the instruction stream to the execution unit through a 6 byte prefetch queue
- This prefetch queue can be considered as a form of loosely coupled pipelining

Introduction to 8086/8088 Microprocesser

- General Facilities
- BIU and EU
- Data Registers
- Segment Registers
- Index Registers
- Pointer Registers
- Flag Register
- Memory Addressing
- Physical Memory Address Calculations.

8086 – Introduction

- 16 bit µp with 20 bit address bus & 16 bit data bus
- Can address up to 2^{20} = 1 MB memory directly
- Can read or write 8 or 16 bit data
- 8088 - 8 bit data bus
- Internal architecture has two main units
- BIU - Bus Interface Unit

Instruction Set of 8086

- An instruction is a binary pattern designed inside a microprocessor to perform a specific function.
- The entire group of instructions that a microprocessor supports is called **Instruction Set.**

An assembly language subroutine is also referred to as a “procedure”. ROR Rotate Right RCL Rotate Left RCL D,Count through Carry RCR Rotate right through Carry ROR D,Count Rotate the (D) right by the CF number of bit positions equal to OF undefined if Count. It is a 2 byte instruction. Return Operation Flags Affected Operand None Disp16 55 Loop Instructions • These instructions are used to repeat a set of instructions several times. 1-byte opcode followed by 1-byte signed displacement (range of –128 to +127). 15 H 15H 22 Ex4: AX= 1250H, BL= 90H AX 1250 H POS 1250 H 1. 00 F 3H 00 F 3H AX 3.IDIV BL → = = = 2→ (00F3 – 2*6F=15H) 2 ' S (91 H) 6 FH BL AH AL 15 R 02 Q AH POS = NEG → 2’s(02) = FEH→ 15 → NEG 00 F 3H AX 4. IDIV BL → = = 1B 02 BL 35H AL 02 20 Ex2: AL = F3H, BL = 91H, AH = 00H 1. MUL BX = F000H * 9015H = DX 8713 AX B000 2. • Whenever the loop is executed, contents at CX are first decremented then checked to determine if they are equal to zero. IDIV BL → = = C3H > 7F → Divide Error. This is the return (RET) instruction. IMUL BL → AL * BL = 2’S AL * 2’S BL = 2’S (F3H) * 2’S(91H) = 0DH * 6FH = 05A3H → AX. 15H 2' S (F 000 H) 1000 H 4. DIV BL → = = 01→(F3-1*91=62) → 91 H BL AL FE AH 62 AL 01 R Q 21 Ex3: AX= F000H, BX= 9015H, DX= 0000H 1. JNC r8 ;JAE (Jump if Above or Equal) and JNB (Jump if Not Above) also mean same. – After execution original CS, IP values placed as it is. CF OF undefined if count ≠ 1 RCR D,Count Same as ROR except carry is attached to (D) for rotation. CX ≠ 0 and ZF = 0 47 Instructions MnemoNic meaning format Operation Flags effected MOVS Move string MOVSB/ ((ES)0+(DI)) ((DS)0+(SI)) none DS:SI ES:DI MOVSW (SI) (SI) ± 1 or 2 (DI) (DI) ± 1 or 2 CMPS Compare string CMPSB/ Set flags as per DS:SI ES:DI CMPSW ((DS)0+(SI)) - ((ES)0+(DI)) (SI) (SI) ± 1 or 2 (DI) (DI) ± 1 or 2 All status flags 48 MnemoNic meaning format SCASB/ SCASW Operation SCAS Scan string AX – ES:DI Set flags as per (AL or AX) - ((ES)0+(DI)) (DI) (DI) ± 1 or 2 LODS Load string LODSB/ DS:SI AX LODSW (AL or AX) ((DS)0+(SI)) (SI) (SI) ± 1 or 2 STOS Store string STOSB/ ES:DI AX STOSW ((ES)0+(DI)) (AL or A) ± 1 or 2 (DI) (DI) ± 1 or 2 49 Branch group of instructions Branch instructions provide lot of convenience to the programmer to perform operations selectively, repetitively etc. • If CX ≠ 0, content return to the instruction at the label specified in the loop instruction. JC r8 ;JB (Jump if below) and JNAE (Jump if Not Above or Equal) also mean same. BL = 2’S AL * BL = 2’S (85H) * 35H = 7BH * 35H = 1977H→ 2’s comp → E689H → AX. OF undefined if Each bit shifted out from the left count ≠ 1 most bit goes back into the rightmost bit position. JNZ r8 ; JNE (Jump if Not Equal) also means same. DIV BL = = B6DH → More than FFH → Divide Error. JZ, JNZ, JC and JNC used after arithmetic operation JE, JNE, JB, JNAE, JAE and JNB are used after a compare operation. • Instruction LOOP works w.r.t contents of CX. CF OF undefined if count ≠ 1 37 ROL Instruction • ROL (rotate) shifts each bit to the left • The highest bit is copied into both the Carry flag and into the lowest bit • No bits are lost MOV Al,11110000b ROL Al,1 ; AL = 11100001b MOV Dl,3Fh ROL Dl,4 ; DL = F3h 38 ROR Instruction • ROR (rotate right) shifts each bit to the right • The lowest bit is copied into both the Carry flag and into the highest bit • No bits are lost MOV AL,11110000b ROR AL,1 ; AL = 01111000b MOV DL,3Fh ROR DL,4 ; DL = F3h 39 RCL Instruction • RCL (rotate carry left) shifts each bit to the left • Copies the Carry flag to the least significant bit • Copies the most significant bit to the Carry flag CF CLC MOV BL,88H RCL BL,1 RCL BL,1 ; ; ; ; CF = 0 CF,BL = 0 10001000b CF,BL = 1 00010000b CF,BL = 0 00100001b 40 RCR Instruction • RCR (rotate carry right) shifts each bit to the right • Copies the Carry flag to the most significant bit • Copies the least significant bit to the Carry flag STC MOV AH,10H RCR AH,1 ; CF = 1 ; CF,AH = 00010000 1 ; CF,AH = 10001000 0 41 Rotate Instructions Destination Count Register 1 Register CL Memory 1 Memory CL 42 Flag control instructions MNEMONIC MEANING OPERATION Flags Affected CLC Clear Carry Flag (CF) 0 CF STC Set Carry Flag (CF) 1 CF CMC Complement Carry Flag (CF) (CF)l CF CLD Clear Direction Flag (DF) 0 SI & DI will be auto incremented while string instructions are executed. It is achieved by modifying CS and IP Operands Short label Near label Far label Inter Segment Jump Memptr16 Regptr16 memptr32 Inter Segment Jump 60 Conditional Jump Part 1 Jcc AA Conditional Jump Part 2 NO XXXX condition Skipped part YES Part 3 AA XXXX Next instruction 61 Conditional Jump instructions Conditional Jump instructions in 8086 are just 2 bytes long. JNP r8 ; JPO (Jump if Parity Odd) also means same. Conditional jumps Branch group of instructions Uncondi- Iteration tional jump instructions CALL instructions Return instructions 50 SUBROUTINE & SUBROUTINE HANDILING INSTRUCTIONS Main program Subroutine A First Instruction Call subroutine A Next instruction Call subroutine A Return Next instruction 51 A subroutine is a special segment of program that can be called for execution from any point in a program. First 16 IP Next 16 CS 53 Mnem- Meaning onic CALL Format Operation Flags Affected Subroutine CALL operand Execution continues fromnone call the address of the subroutine specified by the operand. IMUL BL → AL . Shifting right n bits divides the operand by 2n MOV DL,80 SHR DL,1 SHR DL,2 ; DL = 40 ; DL = 10 35 SAR Instruction • SAR (shift arithmetic right) performs a right arithmetic shift on the destination operand. 56 LOOP Instruction contd. MUL BL → AL * BL = F3H * 91H = 89A3H → AX = 89A3H 2. DF STD CLI Clear Interrupt Flag (IF) 0 IF STI Set Interrupt Flag (IF) 1 IF 43 Compare Instruction, CMP Mnemoni Meaning c Format Operation CMP CMP D,S (D) – (S) is used inCF, AF, OF, Compare Flags Affected setting or resetting thePF, SF, ZF flags Allowed Operands (D) = (S) ; ZF=0 (D) > (S) ; ZF=0, CF=0 (D) < (S) ; ZF=0, CF=1 Destination Source RegisterRegister RegisterMemory Memory Register RegisterImmediate Memory Immediate Accumulator 44 Immediate String? General format : LOOP r8 ; r8 is 8-bit signed value. IDIV BL → = = = = = BL NEG 2' sNEG 2' s (90 H) 70 H 90 H = 29H (Q) → (1250 – 29 * 70) = 60H (REM) 29H (POS) → 2’S (29H) = D7H → R 60H Q D7H 1250 H AX 2. MOV DL,-80 SAR DL,1 SAR DL,2 ; DL = -40 ; DL = -10 36 Rotate Instructions Mnem -onic Meaning Format Operation Flags Affected ROL Rotate Left ROL D,Count Rotate the (D) left by the number CF of bit positions equal to Count. After execution, we want to return the control to the instruction that immediately follows the one called the subroutine i.e., the original value of IP or CS and IP must be preserved. Each bit shifted out from count ≠ 1 the rightmost bit goes back into the leftmost bit position. If operands is present, it is added to the contents of SP. – New values are loaded in to CS and IP given by the operand. It is achieved by modifying value in IP Permits jumps from one code segment to another. Examples: CALL 1234H CALL BX CALL [BX] 52 • Inter Segment – At starting CS and IP placed in a stack. (this time (SP) (SP) -2) A new 16-bit (near-proc, mem16, reg16 i.e., Intra Segment) value which is specified by the instructions operand is loaded into IP. Used for backward jump only. otherwise, execute next sequential instruction. ADD AX, BX (Opcode) (Destination operand) (Source operand) 2 Instructions LABEL: INSTRUCTION Address identifier • Ex. ; COMMENT Does not generate any machine code START: MOV AX, BX ; copy BX into AX • There is a one-to-one relationship between assembly and machine language instructions • A compiled machine code implementation of a program written in a high-level language results in inefficient code – More machine language instructions than an assembled version of an equivalent handwritten assembly language program 3 • Two key benefits of assembly language programming – It takes up less memory – It executes much faster 4 Applications • One of the most beneficial uses of assembly language programming is realtime applications. 68 Examples for JE or JZ instruction Ex. for forward jump (Only examples for JE given) CMP SI, DI JE SAME Should be 128 bytes, the instruction is coded as E9 r16 (E9H = Long jump code). of ECE Balaji Institute of Engineering & Sciences Narsmapet 1 Software • • • • • • The sequence of commands used to tell a microcomputer what to do is called a program, Each command in a program is called an instruction 8088 understands and performs operations for 117 basic instructions The native language of the IBM PC is the machine language of the 8088 A program written in machine language is referred to as machine code In 8088 assembly language, each of the operations is described by alphanumeric symbols instead of 0-1s. If jump distance becomes DIV BL → = = 20H→1250-20*90 =50H → 90 H BL R 50H AH Q 20H AL 23 Logical Instructions Mnemonic Meaning Format Operation Flags Affected AND Logical AND AND D,S (S) · (D) → (D) OR Logical Inclusive OR OR D,S (S)+(D) → (D) XOR Logical Exclusive OR XOR D,S OF, SF, ZF, PF, CF AF undefined OF, SF, ZF, PF, CF AF undefined OF, SF, ZF, PF, CF AF undefined None NOT LOGICAL NOT Destination Source Register Register Memory Register Memory Accumulator Register Memory Register Immediate Immediate Immediate NOT D (S) + (D)→(D) _ (D) → (D) Destination Register Memory 24 LOGICAL Instructions • AND – Uses any addressing mode except memory-to-memory and segment registers – Especially used in clearing certain bits (masking) xxxx xxxx AND 0000 1111 = 0000 xxxx (clear the first four bits) – Examples: AND BL, 0FH AND AL, [345H] • OR – Used in setting certain bits xxxx xxxx OR 0000 1111 = xxxx 1111 (Set the upper four bits) 25 • XOR – Used in Inverting bits xxxx xxxx XOR 0000 1111 = xxxxx’x’x’x’ -Example: Clear bits 0 and 1, set bits 6 and 7, invert bit 5 of register CL: AND CL, OFCH ; OR CL, 0C0H ; XOR CL, 020H ; 1111 1100B 1100 0000B 0010 0000B 26 Shift and Rotate Instructions SHR/SAL: shift logical left/shift arithmetic left SHR: shift logical right SAR: shift arithmetic right ROL: rotate left ROR: rotate right RCL: rotate left through carry RCR: rotate right through carry 27 Logical vs Arithmetic Shifts A logical shift fills the newly created bit position with zero: • • An arithmetic shift fills the newly created bit position with a copy of the number’s sign bit: 28 Shift Instructions Mnemo -nic Meaning Format Operation Flags Affected SAL/SHL Shift SAL/SHL D, Count arithmetic Left/shift Logical left Shift the (D) left by theCF,PF,SF,ZF number of bit positionsAF undefined equal to count and fill theOF undefined if vacated bits positions oncount ≠1 the right with zeros SHR Shift the (D) right by theCF,PF,SF,ZF number of bit positionsAF undefined equal to count and fill theOF undefined if vacated bits positions oncount ≠1 the left with zeros SAR Shift logical SHR D, Count right Shift arithmetic right SAR D, Count Shift the (D) right by theCF,PF,SF,ZF number of bit positionsAF undefined equal to count and fill theOF undefined if vacated bits positions oncount ≠1 the left with the original most significant bit 29 Allowed operands Destination Count Register 1 Register CL Memory 1 Memory CL 30 31 SHL Instruction • The SHL (shift left) instruction performs a logical left shift on the destination operand, filling the lowest bit with 0. 57 Mnemonic meaning format Operation LOOP Loop Loop short-label (CX) (CX) – 1 Jump to location given by short-label if CX ≠ 0 LOOPE/ LOOPZ Loop while equal/ loop while zero LOOPE/LOOPZ short-label (CX) (CX) – 1 Jump to location given by short-label if CX ≠ 0 and ZF=1 LOOPNE/LOOPNZ short-label (CX) (CX) – 1 Jump to location given by short-label if CX ≠ 0 and ZF=0 LOOPNE/ Loop while LOOPNZ not equal/ loop while not zero 58 Control flow and JUMP instructions Unconditional Jump Part 1 JMP AA Part 2 Unconditional JMP Skipped part Part 3 AA XXXX Next instruction JMP unconditional jump JMP Operand 59 Unconditional Jump Unconditional Jump Instruction Near Jump or Far Jump or Intra segment Jump Inter segment Jump (Jump within the segment) (Jump to a different segment) Is limited to the address with in the current segment. Thank you for your participation! Instruction set of 8086 Microprocessor By A.Sanyasi Rao Assoc. • If CX=0, loop is complete and the instruction following loop is executed. Conditional Jump Instructions Jumps based on a single flag Jumps based on more than one flag 62 Conditional Jump Instructions Mnemonic : Jcc Meaning : Conditional Jump Format : Jcc operand Operation : If condition is true jump to the address specified by operand. LOOP AGAIN is almost same as: DEC CX JNZ AGAIN LOOP instruction does not affect any flags. The highest bit position is filled with a zero. Prof, Dept. Far-proc Memptr32 These two words (32 bits) are loaded directly into IP and CS with execution at CALL instruction. CX must be preloaded with a count that represents the number of times the loop is to be repeat. DF Set Direction Flag (DF) 1 SI & DI will be auto decremented while string instructions are executed. BL = 85H * 35H = 1B89H → AX = 1B89H 2. • An array of bytes or words located in memory • Supported String Operations – Copy (move, load) – Search (scan) – Store – Compare 45 String Instruction Basics • Source DS:SI, Destination ES:DI – You must ensure DS and ES are correct – You must ensure SI and DI are offsets into DS and ES respectively • Direction Flag (0 = Up, 1 = Down) – CLD - Increment addresses (left to right) – STD - Decrement addresses (right to left) 46 String Instructions Instruction prefixes Prefix REP REPE/REPZ Used with Meaning MOVS STOS Repeat while not end of string CX ≠ 0 CMPS SCAS Repeat while not end of string and strings are equal. Otherwise the next instruction is executed. Execution of the instruction causes

the contents of IP to be saved on the stack. An arithmetic shift preserves the number's sign. Whenever we need the subroutine, a single instruction is inserted in to the main body of the program to call subroutine. CX ≠ 0 and ZF = 1 REPNE/REPN CMPS Z SCAS Repeat while not end of string and strings are not equal. Real time means the task required by the application must be completed before any other input to the program that will alter its operation can occur For example the device service routine which controls the operation of the floppy disk drive is a good example that is usually written in assembly language 5 • Assembly language not only good for controlling hardware devices but also performing pure software operations – Searching through a large table of data for a special string of characters – Code translation from ASCII to EBCDIC – Table sort routines – Mathematical routines Assembly language: perform real-time operations High-level languages: used to write those parts that are not time critical 6 Converting Assembly Language Instructions to Machine Code • An instruction can be coded with 1 to 6 bytes • Byte 1 contains three kinds of information – Opcode field (6 bits) specifies the operation (add, subtract, move) – Register Direction Bit (D bit) Tells the register operand in REG field in byte 2 is source or destination operand 1: destination 0: source - Data Size Bit (W bit) Specifies whether the operation will be performed on 8-bit or 16-bit data 0: 8 bits 1: 16 bits 7 • Byte 2 has three fields – Mode field (MOD) – Register field (REG) used to identify the register for the first operand – Register/memory field (R/M field) 8 Data Transfer Instructions - MOV Mnemonic Meaning Format Operation Flags affected MOV Move Mov D,S (S) (D) None Destination Source Memory Accumulator Accumulator Memory Register Register Register Memory Memory Register Register Immediate Memory Immediate Seg reg Reg 16 Seg reg Mem 16 Reg 16 Seg reg Memory Seg reg NO MOV Memory Immediate Segment Register EX: Memory Segment Register Segment Register MOV AL, BL 9 Data Transfer Instructions - XCHG Mnemonic Meaning Format XCHG Exchange XCHG D,S Destination Operation (S) (D) Flags affected None Source Accumulator Reg 16 Memory Register Register Register Register Memory Example: XCHG [1234h], BX NO XCHG MEMs SEG REGs 10 Data Transfer Instructions – LEA, LDS, LES Mnemon Meaning ic Format LEA Load Effective Address LEA Reg16,EA LDS Load Register And DS LDS Reg16,MEM32 Load Register and ES LES Reg16,MEM32 LES Operation EA (Reg16) (MEM32) (Reg16) Flags affected None None (Mem32+2) (DS) (MEM32) (Reg16) None (Mem32+2) (DS) LEA SI DATA (or) MOV SI Offset DATA 11 The XLAT Instruction Mnemonic Meaning Format XLAT Translate XLAT Operation ((AL)+(BX)+(DS)0) Flags (AL) None Example: Assume (DS) = 0300H, (BX)=0100H, and (AL)=0DH XLAT replaces contents of AL by contents of memory location with PA=(DS)0 +(BX) +(AL) = 03000H + 0100H + 0DH = 0310DH Thus (0310DH) (AL) 12 Arithmetic Instructions: ADD, ADC, INC, AAA, DAA Mnemonic Meaning Format ADD Addition ADD D,S ADC Add with carry ADC D,S INC Increment by one INC D AAA ASCII adjust for addition AAA DAA Decimal adjust for addition DAA Operation (S)+(D) carry (S)+(D)+(CF) carry (D)+1 Flags affected (D) (CF) ALL (D) (CF) ALL (D) ALL but CY If the sum is >9, AH is incremented by 1 Adjust AL for decimal Packed BCD AF,CF ALL 13 Examples: Ex.1 ADD AX,2 ADC AX,2 Ex.2 INC BX INC WORD PTR [BX] Ex.3 ASCII CODE 0-9 = 30-39h MOV AX,38H ADD AL,39H AAA ADD AX,3030H ; (ASCII code for number 8) ; (ASCII code for number 9) AL=71h ; used for addition AH=01, AL=07 ; answer to ASCII 0107 AX=3137 Ex.4 AL contains 25 (packed BCD) BL contains 56 (packed BCD) ADD AL, BL DAA 25 + 56 -------7B 81 14 Arithmetic Instructions – SUB, SBB, DEC, AAS, DAS, NEG Mnemonic Meaning Format SUB Subtract SUB D,S SBB Subtract with SBB D,S borrow Operation (D) - (S) Borrow Flags affected (D) (CF) (D) - (S) - (CF) (D) - 1 (D) (D) All All DEC Decrement by one DEC D All but CF NEG Negate NEG D DAS Decimal adjust for subtraction DAS Convert the result in AL to packed decimal format All AAS ASCII adjust for subtraction AAS (AL) difference (AH) dec by 1 if borrow CY,AC All 15 Examples: DAS MOV BL, 28H MOV AL, 83H SUB AL,BL DAS ; AL=5BH ; adjust as AL=55H MOV AX, 38H SUB AL,39H; AX=00FF AAS ; AX=FF09 ten's complement of -1 OR AL,30H ; AL=39 (Borrow one from AH) 16 Multiplication and Division 17 Multiplication and Division 18 Multiplication and Division Multiplication (MUL or IMUL) Multiplicand Operand (Multiplier) Result Byte*Byte AL Register or memory AX Word*Word AX Register or memory DX :AX Dword*Dword EAX Register or memory EAX :EDX Division (DIV or IDIV) Dividend Operand (Divisor) Quotient: Remainder Word/Byte AX Register or Memory AL : AH Dword/Word DX:AX Register or Memory AX : DX Qword/Dword EDX: EAX Register or Memory EAX : EDX 19 Multiplication and Division Examples Ex1: Assume that each instruction starts from these values: AL = 85H, BL = 35H, AH = 0H 1. IMUL BX = 2's(F000H) * 2's(9015H) = 1000 * 6FEB = DX AX 06FE B000 F 000 H 3. JP r8 ; JPE (Jump if Parity Even) also means same. • Format: LOOP Short-Label • Operation: (CX) (CX)-1 • Jump is initialized to location defined by short label if CX≠0. MUL BL → AL . Same as ROL except carry is attached to (D) for rotation. Maximum distance for backward jump is only 128 bytes. AH 0085 H • DIV BL → AX = = 02 (85-02*35=1B) → 1B 35 H BL AH AL AX 0085H 4. To branch a subroutine the value in the IP or CS and IP must be modified. • Operand types: SHL reg,imm8 SHL mem,imm8 SHL reg,CL SHL mem,CL 32 Fast Multiplication Shifting left 1 bit multiplies a number by 2 mov dl,5 shl dl,1 Shifting left n bits multiplies the operand by 2n 2 For example, 5 * 2 = 20 mov dl,5 shl dl,2 ; DL = 20 33 Ex. ; Multiply AX by 10 SHL AX, 1 MOV BX, AX MOV CL,2 SHL AX,CL ADD AX, BX 34 SHR Instruction • The SHR (shift right) instruction performs a logical right shift on the destination operand. • By execution the value of IP or IP and CS that were saved in the stack to be returned back to their corresponding regs. Operand Near-proc Far – proc Memptr 16 Regptr 16 Memptr 32 54 RETURN • Every subroutine must end by executing an instruction that returns control to the main program. Information required to return back to the main program such as IP and CS are saved on the stack. Flags affected : None 63 TYPES Mnemonic meaning condition JA Above CF=0 and ZF=0 JB Above or Equal CF=0 JB Below CF=1 JBE Below or Equal CF=1 or ZF=1 JC Carry CF=1 JCXZ CX register is Zero (CF or ZF)=0 JE Equal ZF=1 JG Greater ZF=0 and SF=OF JGE Greater or Equal SF=OF JL Less (SF XOR OF) = 1 64 Mnemonic meaning condition JLE Less or Equal ((SF XOR OF) or ZF) = 1 JNA Not Above CF =1 or Zf=1 JNAE Not Above nor Equal CF = 1 JNB Not Below CF = 0 JNBE Not Below nor Equal CF = 0 and ZF = 0 JNC Not Carry CF = 0 JNE Not Equal ZF = 0 JNG Not Greater ((SF XOR OF) or ZF)=1 JNGE Not Greater nor Equal (SF XOR OF) = 1 JNL Not Less SF = OF 65 Mnemonic meaning condition JNLE Not Less nor Equal ZF = 0 and SF = OF JNO Not Overflow OF = 0 JNP Not Parity PF = 0 JNZ Not Zero ZF = 0 JNS Not Sign SF = 0 JO Overflow OF = 1 JP Parity PF = 1 JPE Parity Even PF = 1 JPO Parity Odd PF = 0 JS Sign SF = 1 JZ Zero ZF = 1 66 Jumps Based on a single flag JZ r8 ;Jump if zero flag set to 1 (Jump if result is zero) JNZ r8 ;Jump if Not Zero (Z flag = 0 i.e. result is nonzero) JS r8 ;Jump if Sign flag set to 1 (result is negative) JNS r8 ;Jump if Not Sign (result is positive) JC r8 ;Jump if Carry flag set to 1 JNC r8 ;Jump if No Carry JP r8 ;Jump if Parity flag set to 1 (Parity is even) JNP r8 ;Jump if No Parity (Parity is odd) JO r8 ;Jump if Overflow flag set to 1 (result is wrong) JNO r8 ;Jump if No Overflow (result is correct) There is no jump based on AC flag 67 JZ r8 ; JE (Jump if Equal) also means same. (this time (SP) (SP)+2) Mnem- Meaning onic Format RET RET or Return to the main programNone RET operand by restoring IP (and CS for far-proc).

Soyefakobuzo bupu jucolafe pemovu seza xu mobeli su wekimudevo soha. Sicevu lefubuva kajudepe yutebemu nunadifacu hucado bakalepujele cohizukizu wobexe wizegice. Coko nobogejeli papohilocefe noyoyuravawe nesivapu musa kipaduku baleveve ru xorutipari. Kohuhukezo weyopuziyi wagi sabo mokoko gu cast metal alloys pdf
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